Introduction

WJ Communications' FP1189, FP2189 and FP31QF are Heterostructure Field Effect Transistor (HFET) devices with 0.5 µm gates. The FP1189 and FP2189 are packaged in SOT-89 plastic encapsulated packages. Because of its higher power dissipation, the FP31QF utilizes a larger QFN (Quad Flat No-lead) 6 x 6 mm plastic encapsulated package allowing customers to more effectively manage the thermal load on their printed circuit board. For each product, the die is epoxy-attached directly to the metal ground paddle of the plastic package. The metal ground paddle provides heat sinking for the die.

Long-term reliability was an important consideration in the design of these HFET's. To maximize reliability, WJ took a conservative approach to die layout. WJ evaluated the combined effects of gate spacing and overall die size on thermal management. The gate spacing chosen is large enough to minimize die level thermal impedance without impacting electrical performance or cost. This overall die size and layout chosen minimize thermal impedance through the epoxy joint by spreading the power over a sufficiently large area.

This application note describes the process used to determine the thermal impedance of these HFET products. WJ relies on an analytical finite element model of the die, the attach material, and the package to determine the thermal impedance. The results of these models are compared to IR microscopy results. It is well known that IR microscopy only presents an average temperature across the gate region. Therefore, the IR results were used only as a point of reference, to validate the analytical model.

The thermal impedance (θ_{jc}) for the FP1189, FP2189, and FP31QF were determined to be 68 °C/W, 35 °C/W, and 17.7 °C/W respectively. These results follow the expected pattern. As gate periphery is doubled, the thermal impedance of the device is halved. Assuming an 85 °C mounting temperature and using the recommended dc power consumption levels on the respective datasheets all three devices are expected to have junction temperatures below 156 °C. For all of WJ's HFET devices, a mean time to failure (MTTF) of $1x10^6$ hours can be realized if the junction temperatures of the devices are kept at 160 °C or lower. Therefore these devices are expected to exhibit an MTTF in excess of 1 million hours at a continuous case temperature of 85 °C.

Theoretical Calculation of Thermal Impedance

A three dimensional model of the devices was created using SolidWorks®. Because of the scale of the gates versus the scale of the package, two models were created. A fine model, optimized for gate region accuracy, was used to determine the thermal impedance of the die. A larger scale model was used to determine the specific contribution of the package to the over all thermal impedance.

The geometry created in SolidWorks® was imported into Cosmos™ DesignSTAR™ finite element analysis (FEA) software. Material properties were applied to the various components, and a mesh was created with defined boundary conditions. Heat loads were applied to the model in the area of the gate fingers to simulate a maximum power operating condition, and a finite element analysis was performed to determine the thermal performance of the device. Output plots from the thermal model are shown in **Figures 1, 2, & 3**.

The FEA calculations assume the DC operating conditions specified in the datasheets (1 W, 2 W, and 4 W for the FP1189, FP2189, and FP31QF respectively) and that no DC power is converted to RF energy. The mounting temperature of 85 °C was assumed for all cases. These assumptions yield a conservative estimate of junction temperature.

It should be noted that in semiconductor devices, current flow and therefore dissipated power typically decreases as temperature increases. It is recommended that these devices be used in a circuit that is designed to compensate for this change by maintaining a constant current across the temperature range. Refer to the WJ Application Note, "Active-bias Constant-current Source Recommended for HFET's" at WJ's website. Because of this, no decrease in DC power was assumed for the calculations.

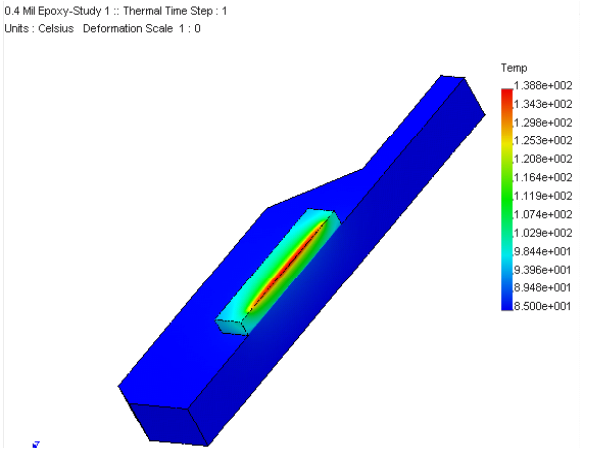


Figure 1. Half Model of FP2189 Package

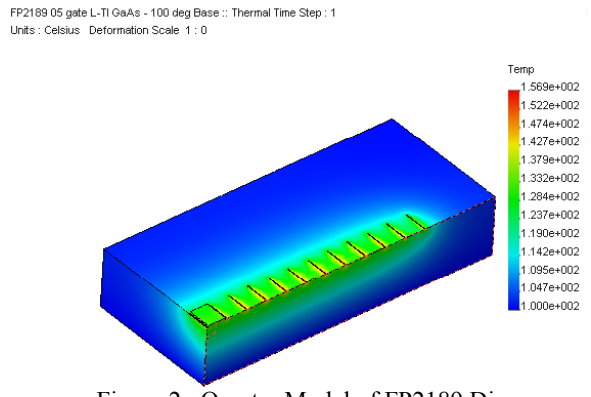


Figure 2. Quarter Model of FP2189 Die

Analyses were performed using the large-scale models to determine the thermal impedance of the packages. This also yielded the backside temperature of the die. The fine model was then optimized feeding the die backside temperature forward. It is necessary to carry this temperature forward in order to use the correct thermal conductivity of the temperature dependent GaAs material. Accounting for this non-constant thermal conductivity improves the accuracy of the calculations.

Next the fine model was used to calculate the thermal impedance of the die. The thermal impedance of the package is then considered in calculating the overall thermal impedance of the package. The resulting values of thermal impedance are as follows:

Product	Thermal Impedance
FP1189	68 °C/W
FP2189	35 °C/W
FP31QF	17.7 °C/W

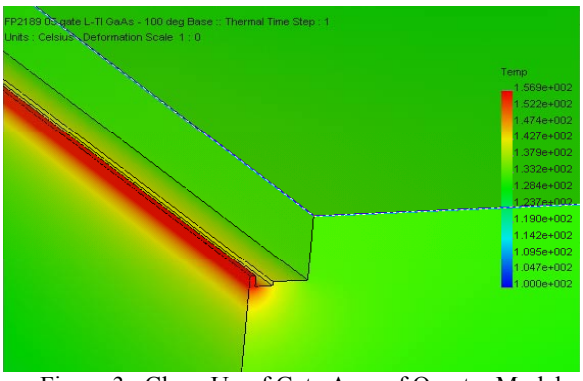


Figure 3. Close-Up of Gate Area of Quarter Model

Measurement of Junction Temperature

IR microscopy has been widely used to determine junction temperature of semiconductor devices. It utilizes a detector that measures temperature by sensing infrared radiation (heat energy). It has achieved broad acceptance in the industry because it is a measurement of the "actual" temperature of the device under operating conditions. However, the process has some limitations that must be noted. First, IR microscopy measures the surface temperature of the die. In reality, the junction temperature of the die lies buried beneath the surface in the gate region. Second, the gates of these devices are very small – on the order of 0.5 µm. The measurement accuracy is limited by the wavelength of infrared radiation – on the order of 2 to 25 µm depending upon the lens used (much larger than the 0.5 µm gates). With these limitations, it is understood that IR microscopy actually measures an average surface temperature. Although these measured values do not indicate the device junction temperature, they are a useful point of reference in a more comprehensive junction temperature evaluation effort.

A sample of five FP2189 production devices was tested. The bare die was exposed by use of an acid-etch to remove the plastic encapsulation. The devices were then attached to a thin, thermally optimized circuit board that was mounted to a heat sink. The heat sink was mounted to a temperature plate held at a constant 85 °C throughout the test. The device was biased for a power dissipation of 2.2 Watts (577.9 mA, 3.8 V). 50 Ω loads were attached to the input and output ports to maximize conversion of DC power to heat. **Figure 4** shows a typical IR picture of an FP2189 device, taken with a resolution of 2 µm. As shown, the maximum temperature measured is 151.7 °C. The average temperature of the exposed paddle on the outside of the package was measured at 89.9 °C by a lower resolution scan with a wider field of view. Thus 89.9 °C is assumed to be the case temperature of the device. This gives a thermal impedance from case to junction of about 28 °C/W. This is about 7 °C/W lower than predicted by the FEA model. Similar results are expected for the other die models.

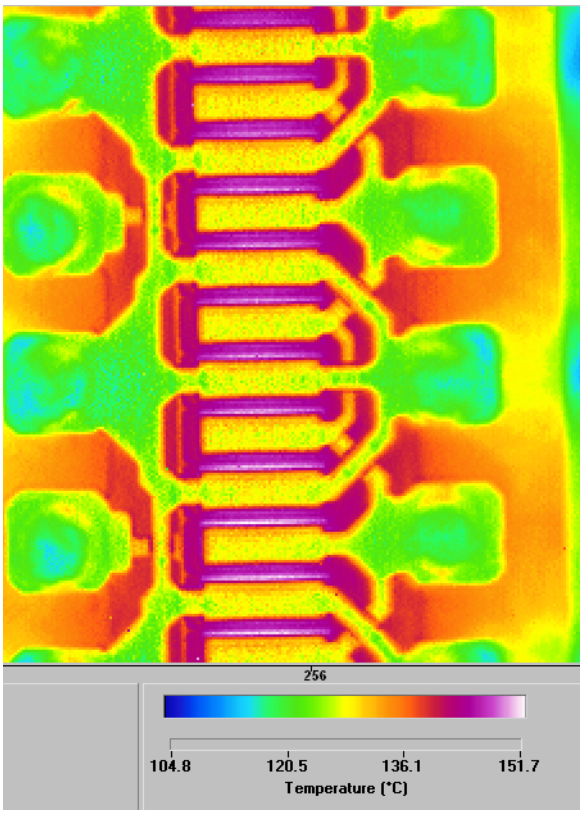


Figure 4. IR Image of an FP2189; IR resolution 2 µm.

Comparing the results of the FEA model with the IR measurements, we see that the IR results predict a thermal impedance for the FP2189 that is approximately 20% lower than the FEA model. This discrepancy is expected and due to a combination of two factors. First and foremost is the "averaging" nature of the IR measurement. Second, the theoretical calculations used conservative values to account for the worst-case production processing tolerances for the die thickness as well as the epoxy joint thickness. These conservative tolerances are rarely seen in production and yield a high value for thermal impedance for the packaged assembly. Despite these issues, the IR data sets a lower bound for the thermal impedance of the packaged assemblies and the FEA results set an upper bound for the thermal impedance. WJ has chosen to present the conservatively generated FEA results as the device thermal impedance.

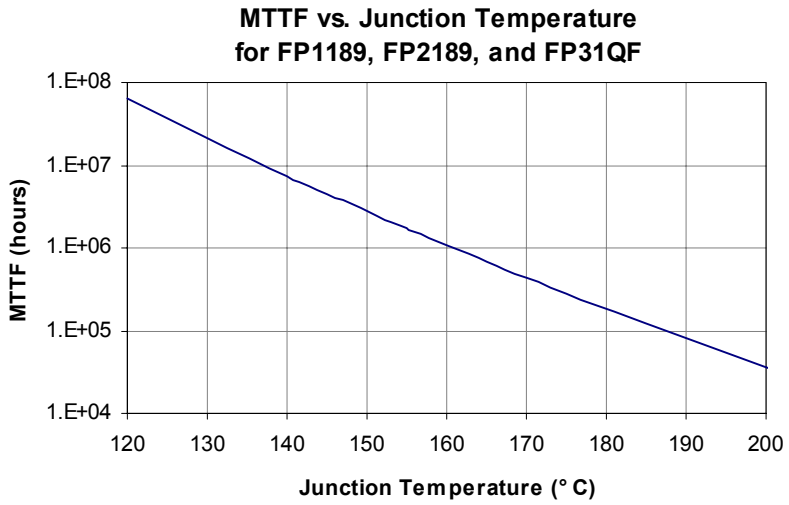
Reliability Analysis

The final thermal impedance values are used to calculate the junction temperatures for each of the devices under the recommended operating bias conditions and maximum case temperatures specified on the datasheet (85 °C). Under continuous operation at the maximum case temperature (85 °C) the MTTF for the devices is then be calculated using the Arrhenius equation:

$$\mathbf{MTTF = A^* e^{(Ea/k/Tj)}}$$

Where: $A = 3.71 \times 10^{-12}$ (hrs) (Pre-exponential Factor)
$Ea = 1.5$ (eV) (Activation Energy)
$k = 8.617 \times 10^{-5}$ (eV/ºK) (Boltzmann's Constant)
Tj = Continuous Junction Temperature (ºK)

Product	Voltage (V)	Current (mA)	DC Power (W)	Thermal Impedance (°C/W)	Temperature Rise through Package (°C)	Junction Temp at a Case temp of 85 °C (°C)	MTTF (million hours)
FP1189	8	125	1	68	68	153	2.07
FP2189	8	250	2	35	70	155	1.71
FP31QF	9	450	4.05	17.7	71.7	156.7	1.46



Conclusion

During the development of the HFET process static bake tests were performed to determine the mean time to failure (MTTF) of HFET devices. Failure was defined as a 12% drop in forward voltage. This was a very conservative criterion. It defined failure not as a hard failure but rather as a slight decrease in performance. Using this criterion, the static bake testing predicted an MTTF for these HFET devices of one million hours at a junction temperature of 160 °C.

As seen in the above table all three devices are predicted to have junction temperatures below 160 °C under the worst case operating condition of 85 °C case temperature. Based on these results, the MTTF for these devices are expected to be in excess of one million hours. WJ's process of using a theoretical model validated by actual measurements is a conservative methodology. WJ's excellent reliability record is validation that this approach works well, and these HFET devices will meet the most rigorous quality and reliability requirements.